Remarks

This REQUEST FOR CONTINUED EXAMINATION and RESPONSE is in reply to the Office Action mailed September 7, 2005. A Petition for Extension of Time is submitted herewith, together with the appropriate fee. No fee is due for the addition of new claims.

I. Summary of Examiner's Rejections

Prior to the Office Action mailed September 7, 2005, Claims 1-24 were pending in the Application. In the Office Action, the drawings were objected to as failing to comply with the requirements of 37 C.F.R. 1.121(d). Claims 1-15 and 19-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al. (U.S. Patent No. 6,477,683, hereafter Killian), in view of Mendel (U.S. Patent No. 6,080,204), and further in view of Havens (U.S. Patent No. 6,345,240). Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Rajsuman (U.S. Patent No. 6,678,645). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of MicroSim (*"MicroSim Pspice A/D & Basics + Circuit Analysis Software User's Guide"*, Version 8.0, June 1997, hereafter MicroSim). Claim 24 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Kang et al.(*"CMOS Digital Integrated Circuits, Analysis and Design"*, Chapter 4, Second Edition, WCB/McGraw Hill, 1999, hereafter Kang).

II. Summary of Applicant's Amendment

The present Response amends Claims 1 and 8-10; cancels Claim 18 and 24; and adds new Claim 25-27, leaving for the Examiner's present consideration Claims 1-17, 19-23 and 25-27. Reconsideration of the Application, as amended, is respectfully requested.

Applicant respectfully reserves the right to prosecute any originally presented or canceled claims in a continuing or future application.

III. Objections to the Drawings

In the Office Action mailed September 7, 2005, the drawings were objected to as failing to comply with the requirements of 37 C.F.R. 1.121(d). In particular, the drawings were objected to for the use of hand-written annotations. Accordingly, enclosed herewith are replacement drawing sheets for Figures 1-4. Subject to the approval of the Examiner, Applicant respectfully requests that the original drawing sheets be replaced with those enclosed herewith. Applicant respectfully submits that the replacement drawing sheets correct informalities in the drawings as originally filed, and that no new matter is being added.

IV. Claim Rejections under 35 U.S.C. §103(a)

In the Office Action mailed September 7, 2005, Claims 1-15 and 19-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (U.S. Patent No. 6,477,683), in view of Mendel (U.S. Patent No. 6,080,204), and further in view of Havens (U.S. Patent No. 6,345,240). Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Rajsuman (U.S. Patent No. 6,678,645). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of MicroSim. Claim 24 was rejected under 35 U.S.C. 103(a) as being unpatentable over Killian and Mendel, and further in view of Kang.

Claim 1

Claim 1 has been amended by the present Response to more clearly define the embodiment therein. As amended, Claim 1 defines:

> *1. (Currently Amended) A method of simultaneously optimizing performance characteristics in circuit synthesis, comprising the steps of:*
>
> *(a) receiving an initial set of design parameters for a circuit to be synthesized;*
>
> *(b) invoking a simulation script to determine which synthesis models should be used with the circuit and to set ranges for any test benches;*
>
> *(c) generating sets of circuit parameters for each performance characteristic of the circuit;*

(d) automatically creating a plurality of test benches, wherein each of the plurality of test benches emulates test circuitry external to the circuit;

(e) simultaneously passing in parallel each set of circuit parameters through a circuit model as specified by the simulation script;

(f) simultaneously running in parallel a simulation of each circuit model on the plurality of test benches in order to measure performance of the circuit model using the set of circuit parameters;

(g) optimizing the circuit synthesis, including receiving the performance measurements for each simulation and determining for which performance characteristics the a specifications are met, and, for those analyses where the specifications are not met then generating new circuit parameter values and repeating steps(c) through (g); and

(h) outputting the final set of circuit parameters for the circuit.

Claim 1, as currently amended, defines the embodiment therein as receiving an initial set of design parameters for a circuit; invoking a simulation script to determine which synthesis models should be used; generating sets of circuit parameters for each performance characteristic; automatically creating a plurality of test benches; simultaneously passing in parallel each set of circuit parameters through a circuit model; and simultaneously running a simulation of each circuit model on the plurality of test benches. The circuit synthesis is then optimized by receiving the performance measurements and determining for which performance characteristics the specifications are met. For those analyses where the specifications are not met the process is repeated. Applicant respectfully submits that these features are not disclosed by the cited references.

The advantages of the embodiment defined by Claim 1 include that it allows for simultaneously optimizing multiple performance characteristics in a circuit synthesis, which results in an overall shorter synthesis time. A simulation script provides necessary parameters such as the circuit parameters of the circuit being synthesized, and sets up appropriate test bench ranges. The system automatically generates a plurality of test benches that may be modified for each of a specified set of conditions. Simulations are then run in parallel for each circuit model on the test benches. Since multiple test benches are used, the synthesis can be simulated for a wide variety of possible scenarios in a shorter time than if each test bench were run serially.

Killian discloses an automated processor generation system for designing a configurable processor and method for the same. In particular, Killian discloses providing an automated processor generation system which uses a description of customized processor instruction set options and extensions in a standardized language to develop a configured definition of a target instruction set, a Hardware Description Language description of circuitry necessary to implement the instruction set, and development tools such as a compiler, assembler, debugger and simulator which can be used to generate software for the processor and to verify the processor. Implementation of the processor circuitry can be optimized for various criteria such as area, power consumption and speed. Once a processor configuration is developed, it can be tested and inputs to the system modified to iteratively optimize the processor implementation. (Column 6, lines 51-64).

However, Applicant respectfully submits that Killian does not appear to teach that any of the steps can be performed simultaneously. Instead, Killian appears to follow the traditional process of performing each step in a serial fashion, in which a first type of analysis is performed using a set of circuit parameters, a circuit model, and a test bench for a first simulation. Performance is then measured for that analysis. A second type of analysis is performed using another set of circuit parameters, another circuit model, and another test bench for a second simulation. Since this is a serial process, each individual simulation must be completed before the next simulation in that set can begin.

Mendel discloses a method and apparatus for compiling an electronic circuit design by contemporaneously bipartitioning the electronic circuit design using parallel processing. Mendel discloses that "compilation tasks" can be identified and performed in isolation from the remainder of a large "compilation project". When one of these stand alone compilation tasks is identified, it can be temporarily segregated and performed by one or more processors which are not working on other tasks. Simultaneously, the remainder of the project compiles under one or more other processors. (Column 4, lines 25-35). Mendel provides examples of how a compilation project can be partitioned, including (a) between full independent compilations of one or more electronic designs; (b) between entities within a logical hierarchical design; (c) between regions of one or more

target hardware devices; and (d) by defining tasks based upon independent logical regions of a design that are isolated from one another by registers. (Column 4, line 47 - Column 5, line 36).

However, it appears from the above description that Mendel requires that the "compilation tasks" be separable in order for them to be segregated and performed by separate processors. According to Mendel, compilation tasks are separable if, for example, they are different electronic designs; different entities within a logical hierarchical design; or different regions of one or more target hardware devices. In this manner, Mendel differs from the present invention in that the tasks performed herein are not amenable to being segregated. Furthermore, the present invention is directed towards the parallel simulation and synthesis of a single circuit, rather than towards the synthesis of two or more circuits that are temporarily separable but will eventually fit within a single hierarchy or on a single target hardware device. The embodiment defined by Claim 1 assists in synthesizing the circuit by optimizing the design against a plurality of test benches, and applying those test benches in a parallel fashion, to shorten the simulation time. The simultaneous passing of each said set of circuit parameters through a respective circuit model is not itself segregated, since doing so would defeat the purpose of running a simulation of each circuit model on the plurality of test benches in order to optimize the circuit over all the test benches.

As described in Applicant's Specification, additional processors could be used to perform the process for multiple circuit models at the same time, but this is an aspect of other embodiments, and is not the focus of Claim 1, in which the optimizer receives the performance measurements for each of the simulations, and determines for which performance characteristics the specifications are met. For those analyses where the specifications are not met the process is repeated. Thus, the process of determining for which performance characteristics the specifications are met is not itself segregated.

Havens discloses a simulation task generator that reduces effort and time required for a user to prepare for a parallel simulation. The simulation task generator receives a request from the user which specifies ranges of parameters that are desired for a particular parallel simulation. The simulation task generator determines a specific combination of parameters which corresponds to each simulation task. The simulation task generator may also assign estimated processor and resource requirements for each of the simulation tasks. (Column 1, lines 39-51).

In the Office Action mailed September 7, 2005, Havens was described as disclosing a simulation task generator that receives a range of parameters desired for a particular parallel simulation. However, as described above, the present invention does not require a user to specify ranges of parameters that are desired for a particular parallel simulation, nor does it require the specification of separable simulation tasks, or an estimated processor and resource requirement for each of those simulation tasks. As such, Applicant respectfully submits that the technique disclosed by Havens is not generally applicable to the problem of simultaneously running in parallel a simulation of each circuit model on a plurality of test benches, in order to measure performance of the circuit model using a set of circuit parameters.

In view of the above comments, Applicant respectfully submits that Claim 1, as currently amended, is neither anticipated by nor obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claim 10

The comments provided above with respect to Claim 1 are hereby incorporated by reference. Claim 10 has been similarly amended to more clearly define the embodiment therein. For similar reasons as provided above with respect to Claim 1, Applicant respectfully submits that Claim 10, as amended, is likewise neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested.

Claims 1-9, 11-17 and 19- 23

Claims 1-9, 11-17 and 19-23 are not addressed separately but it is respectfully submitted that these claims are allowable in view of the comments provided above. Applicant respectfully submits that Claims 1-9, 11-17 and 19-23 are similarly neither anticipated by, nor obvious in view of the cited references, and reconsideration thereof is respectfully requested. It is also submitted that these claims also add their own limitations which render them patentable in their own right. Applicant respectfully reserves the right to argue these limitations should it become necessary in the future.

Claims 18 and 24

Claims 18 and 24 have been canceled by the present Response, rendering moot the rejection of these claims.

V. Additional Amendments

Claims 25-27 have been newly added by the present Response. Applicant respectfully requests that new Claims 25-27 be included in the Application and considered therewith.

VI. Conclusion

In view of the above amendments and remarks, it is respectfully submitted that all of the claims now pending in the subject patent application should be allowable, and reconsideration thereof is respectfully requested. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. §1.136 for extending the time to respond up to and including March 7, 2006.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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By: _____

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